

**AMENDMENT AND RESPONSE**

Serial Number: 09/135,413

Filing Date: August 14, 1998

Title: METHOD FOR OPERATING A DEAPROM HAVING AN AMORPHOUS SILICON CARBIDE GATE INSULATOR

Page 2  
Dkt: 303.354US2

*37* 36  
65.(New) The method of claim 64 wherein:

programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode;

erasing the floating gate transistor comprises erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts; and

further comprising refreshing the charge placed on the floating gate electrode at regular time intervals.

*37* 38  
66.(New) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV;

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate; and  
refreshing the charge placed on the floating gate electrode.

*39* 38  
67.(New) The method of claim 66 wherein:

programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode;

refreshing the charge comprises refreshing the charge placed on the floating gate electrode at regular time intervals; and

further comprising erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

*40*  
68.(New) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between

the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV;

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate;

refreshing the charge placed on the floating gate electrode; and

erasing the floating gate transistor.

41  
69.(New) The method of claim 68 wherein:

programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode;

refreshing the charge comprises refreshing the charge placed on the floating gate electrode at regular time intervals; and

erasing the floating gate transistor comprises erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

42  
70.(New) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor;

reading the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

43  
71.(New) The method of claim 70 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor;

reading the floating gate transistor comprises reading the floating gate transistor by detecting current in the floating gate transistor;

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Page 4

Dkt: 303.354US2

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling; and

further comprising refreshing the floating gate transistor at regular time intervals.

*44*  
72.(New) A method for operating a floating gate transistor comprising:

*E2*  
*(continued)*  
programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor;

refreshing the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

*45*  
73.(New) The method of claim 72 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor;

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling;

refreshing the floating gate transistor comprises refreshing the floating gate transistor at regular time intervals; and

further comprising reading the floating gate transistor by detecting current in the floating gate transistor.

*46*  
74.(New) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor;

refreshing the floating gate transistor;

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Page 5

Dkt: 303.354US2

reading the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

2  
(continued)  
47

28.(New) The method of claim 74 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor;

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling; and

refreshing the floating gate transistor comprises refreshing the floating gate transistor at regular time intervals; and

reading the floating gate transistor comprises reading the floating gate transistor by detecting current in the floating gate transistor.

**REMARKS**

In response to the Office Action mailed December 13, 1999, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 19-21, 28-38, and 43-63 are pending in the application. Claims 19-21, 28-38, and 43-63 are rejected. Claim 29 has been amended to correct for antecedent basis only, and was not amended in response to the rejection of the claims. Claims 64-75 have been added. No new matter has been added.

*Information Disclosure Statements*

The applicant submitted an Information Disclosure Statement on August 14, 1998.

Supplemental Information Disclosure Statements were filed on October 28, 1998, June 25, 1999, and December 8, 1999. The applicant respectfully requests that these Information Disclosure Statements be entered and the documents listed on the attached Forms 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further